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PAGE 1 OF 1

APPLICANT(S)

Barinder Singh Rai, et al.

FILING DATE

Herewith

GROUP

Not Yet Assigned

U.S. PATENT DOCUMENTS

E.I.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
AF	AA 2002/0135817	9/26/02	Wang			
AF	AB 6,401,186	6/4/02	Blodgett			
AF	AC 6,370,611	4/9/02	Callison, et al.			
AF	AD 6,219,745	4/17/01	Strongin, et al.			
AF	AE 6,075,740	6/13/00	Leung			
AF	AF 5,883,855	3/16/99	Fujita			
AF	AG 5,761,706	6/2/98	Kessler, et al.			
AF	AH 5,659,713	8/19/97	Goodwin, et al.			
AF	AI 5,499,355	3/12/96	Krishnamohan, et al.			
AF	AJ 5,461,718	10/24/95	Tatosian, et al.			
AF	AK 5,146,582	9/8/92	Begun			

FOREIGN PATENT DOCUMENTS

E.I.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
AF	AL 11-65920	3/9/99	Japan			Abstract
	AM					
	AN					
	AO					
	AP					
	AQ					

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

AF	AR	Toshio Sunaga, et al., "An Eight-Bit Prefetch Circuit for High-Bandwidth DRAMS's", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 32, No. 1, January 1997, pp. 105-110.
AF	AS	Toshio Sunaga, et al., "A Full Bit Prefetch Architecture for Synchronous DRAM's", <i>IEEE Journal of Solid-State Circuits</i> , Vol. 30, No. 9, September 1995, pp. 998-1005
AF	AT	Thomas Gleeup, et al., "Memory Architecture for Efficient Utilization of SDRAM: A Case Study of the Computation/Memory Access Trade-Off", <i>Proceedings of the Eighth International Workshop on Hardware/Software Codesign</i> , 2000, pp. 51-55
EXAMINER		DATE CONSIDERED 03/13/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.